

third output end, and the stage of the plurality of stages may further include a fourth output transistor including a control end connected to the first node, a first end connected to the clock input end, and a second end connected to the third node.

[0020] In an exemplary embodiment, each of the first control transistor and the second control transistor may include: a first control electrode; an activation portion overlapping the first control electrode; an input electrode overlapping the activation portion; an output electrode overlapping the activation portion; and a second control electrode overlapping the first control electrode and the activation portion, where the second control electrode may receive the second input signal and the fourth input signal which controls threshold voltages of the first control transistor and the second control transistor.

[0021] In an exemplary embodiment, the first input signal and the second input signal may have an enable level during a same period as each other, and the first input signal may be transmitted to the first node through the first control transistor, a threshold voltage of which is lowered by the second input signal.

[0022] In another exemplary embodiment, a gate driving circuit includes a plurality of stages which outputs gate signals to corresponding gate lines, respectively. In such an embodiment, a stage of the plurality of stages includes: a first control transistor including a first end connected to a first end of the stage, a first control end, a second control end, and a second end connected to a first node; a second control transistor including first and second control ends connected to a second input end of the stage to receive a second input signal, a first end connected to the first node, and a second end connected to a first voltage; a first output transistor including a control end connected to the first node, a first end connected to a clock input end of the stage, and a second end connected to a first output end of the stage; and a capacitor connected between the control end of the first output transistor and the second end of the first output transistor.

[0023] In an exemplary embodiment, the stage of the plurality of stages may further include a second output transistor including a first control end connected to the first node, a first end connected to the clock input end, a second end connected to a second output end of the stage to output a carry signal, and a second control end connected to the second output end.

[0024] In an exemplary embodiment, the stage of the plurality of stages may further include an inverter which outputs a signal synchronized to a clock signal of the clock input end to a second node during a period other than a period during which the carry signal is output, wherein the inverter may include at least two transistors connected to a first voltage having a lower voltage level than a low level of the gate signal and back-biased by a back-bias voltage.

[0025] In an exemplary embodiment, the stage of the plurality of stages may further include an inverter which outputs a signal synchronized to a clock signal of the clock input end to a second node during a period other than a period during which the carry signal is output, where the inverter may include a first inverter transistor connected to a first voltage having a lower voltage level than a low level of the gate signal and back-biased by a back-bias voltage, and a second inverter transistor connected to a second voltage having a same voltage level as the low level.

[0026] In another exemplary embodiment, a display device includes: a display portion including a plurality of pixels connected to corresponding gate lines; and a gate driver including a plurality of stages which outputs gate signals to the corresponding gate lines. In such an embodiment, a stage of the plurality of stages includes: a first control transistor diode-connected between a first input end of the stage and a first node, where the first control transistor is biased by a first input signal of the first input end of the stage, and back-biased by a second input signal of a second input end of the stage; a second control transistor including a control end connected to a third input end to receive a third input signal, a first end connected to the first node, and a second end connected to a first voltage, where the second control transistor is back-biased by a fourth input signal of a fourth input end of the stage; a first output transistor including a control end connected to the first node, a first end connected to a clock input end of the stage, and a second end connected to a first output end of the stage; and a capacitor connected between the control end and the second end of the first output transistor, and the second input signal and the fourth input signal have an enable level during different periods from each other.

[0027] In an exemplary embodiment, the stage of the plurality of stages may further include: a second output transistor including a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a second output end of the stage to output a carry signal; and a third output transistor including a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a third output end of the stage to output a compensation signal, and the second output transistor may be back-biased by the compensation signal.

[0028] In an exemplary embodiment, the stage of the plurality of stages may further include an inverter which outputs a signal synchronized to a clock signal of the clock input end during a period other than a period during which the carry signal is output, and a holding unit which outputs a back-bias voltage to a third output end in response to a signal output from the second node.

[0029] In another exemplary embodiment, a gate driving circuit includes a plurality of stages which outputs gate signals to corresponding gate lines. In such an embodiment, a stage of the plurality of stages includes: a first control transistor diode-connected between a first input end of the stage and a first node, where the first control transistor is biased by a first input signal of the first input end of the stage, and back-biased by a second input signal of a second input end of the stage; a second control transistor including a control end connected to a third input end of the stage to receive a third input signal, a first end connected to the first node, and a second end connected to a first voltage, where the second control transistor is back-biased by a fourth input signal of a fourth input end of the stage; a first output transistor including a control end connected to the first node, a first end connected to a clock input end of the stage, and a second end connected to a first output end of the stage; a capacitor connected between a control end and a second end of the first output transistor; a second output transistor including a control end connected to the first node, a first end connected to the clock input end, and a second end connected to a second output end of the stage to output a carry signal; a first inverter transistor connected to a first voltage